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;; FILENAME: DUALADC\_1.inc

;; Version: 2.2, Updated on 2010/12/27 at 15:27:25

;; Generated by PSoC Designer 5.4.3191

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;; DESCRIPTION: Assembler declarations for the DualADC User Module.

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; Constants for DUALADC\_1 API's.

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; Counter1 Constants

DUALADC\_1\_bfCounter1\_Mask: equ 01h

DUALADC\_1\_bfCounter1\_INT\_REG: equ 0dfh

; Counter2 Constants

DUALADC\_1\_bfCounter2\_Mask: equ 08h

DUALADC\_1\_bfCounter2\_INT\_REG: equ 0dfh

; PWM Constants

DUALADC\_1\_bfPWM16\_Mask: equ 04h

DUALADC\_1\_bfPWM16\_INT\_REG: equ 0dfh

; Power Settings

DUALADC\_1\_bfPOWERMASK: equ 03h

DUALADC\_1\_OFF: equ 00h

DUALADC\_1\_LOWPOWER: equ 01h

DUALADC\_1\_MEDPOWER: equ 02h

DUALADC\_1\_HIGHPOWER: equ 03h

; Parameter Settings

DUALADC\_1\_bNUMBITS: equ 7h

DUALADC\_1\_bCALCTIME: equ 58h

DUALADC\_1\_bMAXRES: equ 0Dh ; Max resolution 13 bits

DUALADC\_1\_bMINRES: equ 07h ; Min resolution 7 bits

DUALADC\_1\_fCOMPARE\_TRUE: equ 08h ; Bit to enable compare True interrupts

; Functionality constants

DUALADC\_1\_fFSW0: equ 10h ; Switch Cap FSW0 switch enable

DUALADC\_1\_NoAZ: equ 01h ; Set if AutoZero is no enabled

DUALADC\_1\_fAutoZero: equ 20h ; Switch Cap AutoZero switch enable

DUALADC\_1\_fDBLK\_ENABLE: equ 01h ; Digital block enable bit

DUALADC\_1\_fPULSE\_WIDE: equ 04h ; Enable wide terminal count pulse.

; fStatus definitions

DUALADC\_1\_fDATA\_READY: equ 10h ; This bit is set when data is available

DUALADC\_1\_bRES\_MASK: equ 0Fh ; This bit while in integrate cycle

; Data Format

DUALADC\_1\_DATA\_FORMAT: equ 0

; Flag in CR2 register mask

DUALADC\_1\_fRES\_SET: equ 01h

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; Register Address Contants for DUALADC\_1

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; TriADC PSoC Block register Definitions

; Integrator1 Block Register Definitions

DUALADC\_1\_bfADC1cr0: equ 90h

DUALADC\_1\_bfADC1cr1: equ 91h

DUALADC\_1\_bfADC1cr2: equ 92h

DUALADC\_1\_bfADC1cr3: equ 93h

; Integrator2 Block Register Definitions

DUALADC\_1\_bfADC2cr0: equ 98h

DUALADC\_1\_bfADC2cr1: equ 99h

DUALADC\_1\_bfADC2cr2: equ 9ah

DUALADC\_1\_bfADC2cr3: equ 9bh

; Counter1 Block Register Definitions

DUALADC\_1\_fCounter1FN: equ 40h

DUALADC\_1\_fCounter1SL: equ 41h

DUALADC\_1\_fCounter1OS: equ 42h

DUALADC\_1\_bCount1: equ 40h

DUALADC\_1\_bPeriod1: equ 41h

DUALADC\_1\_bCompare1: equ 42h

DUALADC\_1\_bCounter1\_CR0: equ 43h

; Counter2 Block Register Definitions

DUALADC\_1\_fCounter2FN: equ 4ch

DUALADC\_1\_fCounter2SL: equ 4dh

DUALADC\_1\_fCounter2OS: equ 4eh

DUALADC\_1\_bCount2: equ 4ch

DUALADC\_1\_bPeriod2: equ 4dh

DUALADC\_1\_bCompare2: equ 4eh

DUALADC\_1\_bCounter2\_CR0: equ 4fh

; PWM16 Block Register Definitions

DUALADC\_1\_bfPWM\_LSB\_FN: equ 44h

DUALADC\_1\_bfPWM\_MSB\_FN: equ 48h

DUALADC\_1\_fPWM\_LSB\_CR0: equ 47h

DUALADC\_1\_fPWM\_MSB\_CR0: equ 4bh

DUALADC\_1\_bPWM\_Count\_MSB: equ 48h

DUALADC\_1\_bPWM\_Count\_LSB: equ 44h

DUALADC\_1\_bPWM\_Period\_MSB: equ 49h

DUALADC\_1\_bPWM\_Period\_LSB: equ 45h

DUALADC\_1\_bPWM\_IntTime\_MSB: equ 4ah

DUALADC\_1\_bPWM\_IntTime\_LSB: equ 46h

DUALADC\_1\_bfPWM\_LSB\_FN: equ 44h

DUALADC\_1\_bfPWM\_MSB\_FN: equ 48h

; end of file DUALADC\_1.inc